WHAT IS CLAIMED IS:

1. An electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

at least one of a first protective transistor provided between the first power-source line and the second power-source line and a second protective transistor provided between the first ground line and the second ground line;

third protective transistors respectively disposed at at least two of a position between the first power-source line and the third power-source line, a position between the first ground line and the third ground line, a position between the first power-source line and the third ground line, and a position between the first ground line and the third power-source line;

fourth protective transistors disposed at at least two of a position between the second power-source line and

the third power-source line, a position between the second ground line and the third ground line, a position between the second power-source line and the third ground line, and a position between the second ground line and the third power-source line; and

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block, wherein

at least one of the first protective transistor and the second protective transistors is disposed in the vicinity of the connection line.

2. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 1, wherein

a distance in each of the first protective transistor and the second protective transistor from a contact hole for connecting an impurity diffusion layer serving as a source and a drain of the protective transistors with a metallic wiring, to a gate of the protective transistor is shorter than a distance in each of the third and fourth protective transistors from a contact hole for connecting an impurity diffusion layer serving as a source and a drain of the protective transistor with a metallic wiring, to a gate of the protective transistor.

3. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 1, wherein:

at each of the first protective transistor and the second protective transistor, a compound layer of silicon and metal is formed on the entirety of a surface between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate; and

at each of the third and fourth protective transistors, a region, where no compound layer of silicon and metal is formed, is provided between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate.

4. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 1, wherein

the distance in each of the first protective transistor and the second protective transistor from the contact hole for connecting the impurity diffusion layer serving as the source and the drain of the protective transistor with a metallic wiring, to the gate of the protective transistor has a minimum value possible in a fabrication process.

5. An electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

first protective transistors respectively disposed at at least two of a position between the first power-source line and the third power-source line, a position between the first ground line and the third ground line, and a position between the first power-source line and the third ground line, a position between the first ground line and the third power-source line;

second protective transistors respectively disposed at at least two of a position between the second power-source line and the third power-source line, a position between the second ground line and the third ground line, a position between the second power-source line and the third ground line, and a position between the second ground line and the third power-source line;

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block; and

at least one of a first resistor whose one end is connected to the first power-source line and whose other end is connected to the second power-source line and a second resistor whose one end is connected to the first ground line and whose other end is connected to the second ground line, wherein

at least one of the first resistor and the second resistor is disposed in the vicinity of the connection line.

6. An electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

at least one of a first protective element provided between the first power-source line and the second power-source line and a second protective element provided between the first ground line and the second ground line;

first protective transistors respectively disposed at at least two of a position between the first power-source line and the third power-source line, a position between the first ground line and the third ground line, a position between the first power-source line and the third ground line, and a position between the first ground line and the third power-source line;

second protective transistors respectively disposed at at least two of a position between the second power-source line and the third power-source line, a position between the second ground line and the third ground line, a position between the second power-source line and the third ground line, and a position between the second ground line and the third power-source line; and

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block, wherein

at least one of the first protective element and the second protective element is disposed in the vicinity of the connection line.

7. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 6, wherein

the first and second protective elements are the third and fourth protective transistors.

8. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 7, wherein

a distance in each of the third protective transistor and the fourth protective transistor from a contact hole for connecting an impurity diffusion layer serving as a source and a drain of the protective transistor with a metallic wiring, to the gate of the protective transistor is shorter than a distance in each of the first protective transistor and the second protective transistor from a contact hole for connecting an impurity diffusion layer serving as a source and a drain of the protective transistor with a metallic wiring, to the gate of the protective transistor.

9. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 7, wherein:

at each of the third protective transistor and the fourth protective transistor, a compound layer of silicon and metal is formed on the entirety of a surface between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate; and

at each of the first and the second protective transistors, a region, where no compound layer of silicon

and metal is formed, is provided between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate.

10. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 7, wherein

the distance in each of the third protective transistor and the fourth protective transistor from an impurity diffusion layer serving as a source and a drain of the protective transistor with a metallic wiring, to the gate of the protective transistor has a minimum value possible in a fabrication process.

11. The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device of claim 6, wherein

the first and second protective elements are resistors.